Remarks:

Applicant appreciatively acknowledges the Examiner's confirmation of receipt of Applicant's claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 17 are presently pending in the application. Claims 1 - 6 and 8 have been amended. New claims 11 - 17 have a been added.

On page 2 of the above-identified Office Action, an information disclosure statement filed February 20, 2002 was objected to. That information disclosure included a German translation of European Patent EP 0683455 B1 to Klingler ("**KLINGLER**"), dated November 22, 1995 and an English translation of a Japanese Patent Abstract JP 63 085 942 A to Inoue ("**INOUE**"), dated April 16, 1988. A copy of U. S. Patent No. 5,819,023, which was found to correspond to **KLINGLER** is included herewith. However, it is not known why the English translation of the **INOUE** abstract was not considered. Applicant is filing the translation of **KLINGLER** and is resubmitting the English abstract for **INOUE** and requesting that they be considered. A form 1449 listing these two references is being provided herewith.

Further on page 2 of the Office Action, the specification was objected to because the title was allegedly non-descriptive. The title has been amended to even more clearly describe the claimed invention.

On page 3 of the Office Action, claims 1 - 10 were rejected as allegedly being indefinite under 35 U.S.C. § 112, second paragraph. More particularly, claims 1 - 4, 6 and 8 were rejected as containing the term "program running unit". This term has been amended to "program operation unit". Support for this change is found on page 5, lines 21 - 26 and page 6, lines 1 - 7.

Additionally on page 3 of the Office Action, claim 5, and claims depending therefrom, were rejected because of the recitation in that claim of the phrases "at least partially connected" in line 3 and "and components that can be stopped by said stopping device". Claim 5 has been amended to address the issues raised in the Office Action. It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph.

Further, on page 4 of the above-identified Office Action, claims 1 - 10 were rejected as allegedly being anticipated

under 35 U.S.C. § 102 by U. S. Patent No. 5,678,003 to Brooks ("**BROOKS**"). Claim 7 was further rejected under 35 U.S.C. § 103(a), as allegedly being obvious over **BROOKS** in view of pages 658 - 659 of *Hennessy*, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann Publishers, 2nd edition ("**HENNESSY**").

Applicant respectfully traverses the above rejections, as they relate to the new and amended claims.

I. Applicant's claimed invention recites limitations neither taught, nor suggested in the cited references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

A. The BROOKS reference neither teaches, nor suggests, among other limitations of Applicant's claim 1, that the stopping device is located on the same chip as program operation unit.

Claim 1, as amended herein, recites:

> "1. A programmable unit, comprising:
>
> at least one program operation unit for running a program;
>
> a stopping device connected to said program operation unit, said stopping device stopping the running of the program by said program operation unit, **said stopping device being located on the same chip as said program operation unit**;

> other components connected to said stopping device, said stopping device also causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated." [emphasis added by Applicant]

As such, claim 1 has been amended to recite that the **stopping device is located on the same chip as the program operation unit.** This is supported in the specification of the present application on page 7, lines 20 - 25, which states:

> "As can be seen from the figure, **the programmable unit under consideration contains** a first program running unit CORE1, **an on-chip debug support (OCDS) module OCDS1** which is associated with the first program running unit CORE1, and a master interface MIF1 which is associated with the first program running unit CORE1, for connection to a bus BUS." [emphasis added by Applicant]

See also, page 1, lines 17 - 20 and page 6, lines 9 - 10.

In connection with the rejection of Applicant's original claim 10, which recites, among other limitations, that the **stopping device is an on-chip debug support module**, the Office Action stated on page 6:

> "Regarding claim 10, Brooks has taught the programmable unit of claim 1, wherein said stopping device is an on-chip debug support module (104 of Figure 2). The Test & Debug Unit disclosed by Brooks encompasses an equivalent function as the OCDS module."

Applicant respectfully traverses the above statement made in the Office Action in connection with claim 10, and

additionally, as the above argument would apply to amended claim 1. Among other limitations of Applicant's claims not taught, the **BROOKS** reference does not teach that the device responsible for stopping the processor is located on-chip with the processor. More specifically, **BROOKS** discloses a method and system for providing a restartable stop in a multiprocessor system wherein the device responsible for stopping the processor(s) is specifically located off-chip. For example, the **BROOKS** reference specifically discloses the use of an external scan interface tool (14 of Fig. 2). In column 4, lines 6 - 17, the **BROOKS** reference states:

> "**The present invention takes advantage of the fact that there is typically a common I/O pin on a microprocessor which is utilized to indicate that the internal processor clocks should be stopped due to a nonmaskable stop or error condition** (i.e., CheckStop_ signal). Through the present invention, **this common pin** is simply switched to a different mode when a private JTAG instruction, mp_ debug, is issued. **By switching the pin in this manner, and also hardwiring this common pin between processors in the multiprocessor system**, each processor in the multiprocessing system can stop code execution in a restartable manner much faster than previously known systems." [emphasis added by Applicant]

It is a ***goal*** of the **BROOKS** reference to use **an external I/O pin to stop the processor.** Clearly, **BROOKS** does not teach or suggest putting the debugging on-chip. To do so would destroy what is taught in **BROOKS**.

In the Office Action, element 104 of **BROOKS** is pointed to as being an on-chip debugging element. Applicant respectfully disagrees that element 104 stops the processor in **BROOKS.** As stated in col. 5, lines 11 - 16 of **BROOKS**:

> "The microprocessor 102 includes a test and debug interface unit (TIU) 104 which is coupled to an instruction flow unit (IFU) 106. The IFU 106 is responsible for instruction dispatch and completion. Within the TIU 104 is an industry standard scan port 110 which includes an instruction set used for test and debug functions."

However, as is made clear in **BROOKS**, in col. 5, lines 17 - 40:

> "The interface between the IFU 106 and TIU 104 includes a plurality of signals. **The soft_ stop_ debug signal 111 informs the IFU 106 that the private JTAG instruction 'soft stop debug' has been issued by the scan interface tool, and the processor is in debug mode.** In the case of an instruction address breakpoint, the processor should not take an interrupt when the breakpoint is reached (as is the case in normal, non-debug mode), but should (a) stop fetching and dispatching instructions (b) complete all outstanding instructions (c) assert the idle signal 113 to the TIU 104 when (a) and (b) are accomplished.
>
> In the case of single instruction dispatch mode, the processor should (a) complete one instruction (b) assert the idle signal 113 to the TIU 104 when (a) is accomplished.
>
> The idle signal 113 informs the TIU 104 that the processor has stopped fetching and dispatching instructions and has completed all outstanding instructions. **The halt signal 115 informs the IFU 106 that the private JTAG instruction 'halt' has been issued by the scan interface tool**, and the processor should (a) stop fetching and dispatching instructions, (b) complete all outstanding instructions, (c) assert the idle signal 113 to the TIU 104 when (a) and (b) are accomplished.

As such, the element responsible for stopping the processor in **BROOKS**, ***is not the TIU 104, but the externally connected scan interface tool 14.*** In the ultimate show of teaching away from Applicant's invention of claim 1, **BROOKS** includes an on-chip debugging circuit **and teaches the use of a different, external component (scan interface tool 14) to stop the processor.**

As such, **BROOKS** clearly fails to teach or suggest Applicant's limitation of claim 1, that the stopping device be on the same chip as the processor that it stops. As such, it is believed that claims 1 - 10 are patentable over the **BROOKS** reference.

B. The BROOKS reference neither teaches, nor suggests, among other limitations of Applicant's claim 11, that the stopping device that stops the program operation unit also stops associated peripherals.

New claim 11, recites:

> "11. (new) A programmable unit, comprising:
>
> at least one program operation unit for running a program;
>
> a stopping device connected to said program operation unit, said stopping device stopping the running of the program by said program operation unit; and
>
> **peripherals connected to said stopping device, said stopping device also causing said peripherals to be stopped,** in addition to stopping said program operation unit with which said stopping device is associated." [emphasis added by Applicant]

As such, Applicant's new claim 11, and all claims depending therefrom, require, among other limitations, that the "**stopping device**" be connected to stop, not only the program operation unit with which the **stopping device** is associated, but also the claimed "**peripherals**". This is supported in the instant application, on page 3, lines 23 - 26, which state:

> "The programmable units according to the invention are distinguished in that **the stopping device can also cause other components of the programmable unit to be stopped**, in addition to the program running unit with which it is associated." [emphasis added by Applicant]

See also, page 10, lines 6 - 10. These **"peripherals"** are defined in the instant specification on page 8, lines 21 - 24, which state:

> "The peripheral units P1 and P2 are, for example, A/D converters, timers, DMA controllers or other units, which can be used in programmable units in addition to one or more program running units, and cooperate with them."

Applicant believes that the **BROOKS** reference fails teach or suggest that **peripherals** are connected to the scan interface tool 14 of that reference, which was shown above in section A) to be the device that stops the processor. In column, 6, lines 23 - 35, **BROOKS** states:

> "After each processor indicates a stop_ req, **the scan interface tool 14 issues a JTAG halt instruction to the system bus arbiter 110, indicating that it should terminate or pause all bus activity normally required**

> **to be snooped, such as direct memory access (DMA) from the I/O subsystem 21, via step 314.** Thereafter, the scan interface tool polls the stop_ req status bit of the system bus arbiter 110 via step 316. Finally when the system bus arbiter 110 indicates stop_ req the scan interface tool stops all functional clocks via the JTAG interface, via step 318. Accordingly, memory coherency of the multiprocessor system has been preserved, and the system is restartable." [emphasis added by Applicant]

As can be seen in the foregoing, the **BROOKS** reference teaches using the scan interface tool 14 to issue a halt instruction to the system bus arbiter 110, **but not to an associated peripheral (i.e. the DMA, itself).**

As such, the **BROOKS** reference fails to teach or suggest, among other limitations of Applicant's claims, "**peripherals connected to said stopping device, said stopping device also causing said peripherals to be stopped.**"

In view of the foregoing, it is believed that Applicant's claim 11, and claims 12 - 17 depending therefrom, are patentable over the **BROOKS** reference.

C. The HENNESSY reference cited against claim 7 in the Office Action, does not cure the failures in the teachings of BROOKS.

The **HENNESSY** reference cited in the Office Action, among other limitations of Applicant's claims, neither teaches, nor suggests: 1) a stopping device located on the same chip as a

program operation unit and connected to the program operation unit, as required by Applicant's claim 1; or 2) peripherals connected to a stopping device, the stopping device also causing said peripherals to be stopped, as required by Applicant's claim 11. As such, **HENNESSY** fails to overcome the failures of the **BROOKS** reference.

II. In view of the foregoing, Applicant's claims are patentably distinguishable over the BROOKS and HENNESSY references, and it is requested that claims 1 - 20 be allowed.

It is accordingly believed that none of the references, whether taken alone or in any combination, either show or suggest the features of Applicant's independent claims 1 and 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all ultimately depend from either claims 1 or 11.

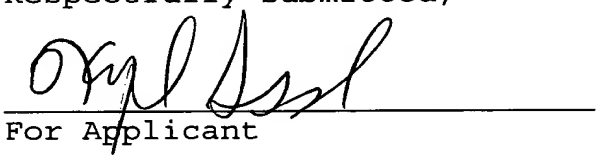
In view of the foregoing, reconsideration and allowance of claims 1 - 17 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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